REMARKS

This response places the above-referenced patent application in better condition for allowance, and therefore, is a proper response after Final pursuant to 37 C.F.R. §1.116.

Claims 36-75 are pending in the application. Claims 36, 46 and 56 are amended as agreed to during the March 3, 2003 interview with Examiner Rose. Examiner Rose stated that such amendments to the independent claims would put the case in form for allowance. Accordingly, Applicant has amended the claims as agreed, and therefore, respectfully requests allowance of independent claims 36, 46 and 56.

Moreover, claims 37-45 and 61-65 are allowable for depending from allowable independent claim 36.

Furthermore, claims 47-55 and 66-70 are allowable for depending from allowable independent claim 46.

Additionally, claims 57-60 and 71-75 are allowable for depending from allowable independent claim 56.

Further, Applicant herewith submits duplicate copies of the Information Disclosure Statement and Form PTO-1449 and the Supplemental Information Disclosure Statement and Form PTO-1449s filed in this application on August 1, 2001 and August 7, 2001, respectively. No initialed copy of the PTO-1449s have been received back from the Examiner. To the extent that the submitted references listed on the Form PTO-1449s have not already been considered, and

the Form PTO-1449s have not been initialed with a copy being returned to Applicant, such examination and initialing is requested at this time, as well as return of a copy of the initialed Form PTO-1449s to the undersigned.

In view of the foregoing, allowance of all pending claims is requested. This application is now believed to be in immediate condition for allowance, and action to that end is respectfully requested. If the Examiner's next anticipated action is to be anything other than a Notice of Allowance, the undersigned respectfully requests a telephone interview prior to issuance of any such subsequent action.

Respectfully submitted,

Dated: 3-3-03

By: _____

D. Brent Kenady
Reg. No. 40,045

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/920,979
Filing Date ..... August 1, 2001
Inventor ..... Monte Manning
Assignee ..... Micron Technology, Inc.
Group Art Unit 2822
Examiner ..... K.L. Rose
Attorney's Docket No. MI22-1698
Title: Thin Film Transistors and Methods of Forming Thin Film Transistors

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO DECEMBER 3, 2002 FINAL OFFICE ACTION PURSUANT TO 37 C.F.R. §1.116

The replacement paragraphs incorporate the following amendments. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

36. (Amended) A thin film transistor comprising:

a variable thickness thin film transistor layer, the transistor layer having a channel region and one of a source region or a drain region elevationally above the channel region, the one region comprising at least a lateral width portion thicker than a lateral width portion of the channel region; and

a gate in lateral proximity to the thin film channel region, the gate comprising an annulus which laterally encircles the laterally proximate thin film channel region.

46. (Amended) A thin film transistor comprising:

a variable thickness thin film transistor layer, the transistor layer having a thin film channel region, a first thin film source/drain (S/D) region and a second thin film S/D region, the first S/D region having a different lateral width thickness than the second S/D region; and

a gate in lateral proximity to the thin film channel region, the gate comprising an annulus which laterally encircles the laterally proximate thin film channel region.

56. (Amended) A thin film transistor comprising:

a first dielectric layer disposed over a semiconductor substrate;

a gate electrode layer disposed over the first dielectric layer;

a second dielectric layer disposed over the gate electrode layer and having an upper surface;

an opening extending from the upper surface to the semiconductor substrate, the opening, in cross-sectional view, having opposing sidewalls;

a gate dielectric layer disposed over a portion of the sidewalls as an annulus, the annulus having a top ~~disposed elevationally below~~ terminating at the upper surface; and

a channel region disposed within the opening, operably adjacent the gate dielectric layer.

-END OF DOCUMENT-